WHAT IS CLAIMED IS:

1. A MOSFET device comprising:

a source and a drain formed on an insulating layer;

a fin structure formed on the insulating layer between the source and the drain, the fin structure including a first region formed in a channel area of the fin structure;

a protective layer formed over at least the first region of the fin structure, the protective layer being wider than the first region; and

a gate formed on the insulating layer around at least a portion of the fin structure.

2. The MOSFET device of claim 1, wherein the first region has a width of about 3 to 6 nm.

3. The MOSFET device of claim 1, wherein the protective layer includes:

an oxide layer, and

a nitride layer formed over the oxide layer.

4. The MOSFET device of claim 3, wherein the oxide layer has a thickness of about 15 nm and the nitride layer has a thickness ranging from about 50 nm to 75 nm.

5. The MOSFET device of claim 1, further comprising:

a dielectric layer formed around at least a channel portion of the fin structure.

6. The MOSFET device of claim 5, wherein the dielectric layer is about 0.6 nm to 1.2 nm thick.

7. The MOSFET device of claim 1, wherein the gate comprises polysilicon.

8. The MOSFET device of claim 1, wherein the MOSFET device is a FinFET.

9. The MOSFET device of claim 1, wherein the gate is formed to include small gate lengths.

10. A method for forming a MOSFET device comprising:

forming a source, a drain, and a fin structure on an insulating layer, portions of the fin structure acting as a channel for the MOSFET;

forming a protective layer above the fin structure;

trimming the fin structure without significantly trimming the protective layer; and

depositing a polysilicon layer to act as a gate area for the MOSFET.

11. The method of claim 10, wherein the fin structure is trimmed by exposing the fin structure to NH4OH.

12. The method of claim 10, wherein forming the protective layer includes:

depositing an oxide layer to a depth of about 15 nm, and

depositing a nitride layer to a depth of about 50 nm to 75 nm.

13. The method of claim 10, further comprising:

depositing a tetraethylorthosilicate (TEOS) layer over the MOSFET device before trimming the fin structure.

14. The method of claim 13, further comprising:

etching away the TEOS layer over the fin structure before trimming the fin structure.

15. The method of claim 13, further comprising:

depositing the polysilicon layer to a thickness ranging from about 50 nm to 70 nm on the TEOS layer.

16. The method of claim 10, wherein trimming the fin structure includes trimming the fin structure to a width of about 3 nm to 6 nm.

17. A device comprising:

a source and drain;

a fin structure formed between the source and the drain, the fin structure including a first region formed in a channel area of the fin structure and a second and third protective region formed adjacent the source and drain, respectively, wherein the first region is narrower than the second and third protective regions; and

a gate formed around at least a portion of the fin structure.

18. The device of claim 17, wherein the first region is approximately 4 to 12 nm thinner than the second and third regions.